SIERRA VIDEO SYSTEMS, INC.

DigiLinx Digital Audio Delay User's Guide

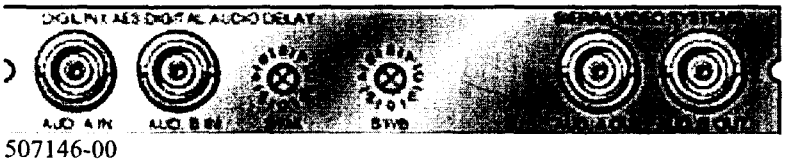
507146-00
507146-10

V 1.4

Introduction

The DigiLinx Digital Audio Delay is a solid state time delay product which accepts two AES or S/PDIF digital audio streams and produces two AES or S/PDIF digital audio streams. The time delay through the product is adjustable from a minimum value of roughly 1 millisecond to a maximum value of 21.8 seconds for 48 KHz sample rate audio (longer for slower sample rates). The incoming signals are normally delayed without any alteration of the bit stream; no compression or ancillary data blanking occurs. Delay is adjustable in (roughly) 1 msec. increments via rear panel controls, direct connection to a Windows computer, or a SmartLinx network control product. Additional features include independent delay control of the two audio streams and sample rate independence between the two audio streams. The product is offered in BNC and 'pluggable' terminal strip I/O versions.

Peripheral Connections



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The rear panel provides the following signal connections to the user:

AUD. A IN - This BNC or terminal strip connector serves as one of two AES or S/PDIF digital signal stream inputs to the product. Signals applied here are fed to the time delay and to the clock generation circuitry for the module. In either connector version, the signal can be balanced, unbalanced, 75 Ohm terminated, or 110 Ohm terminated. Signals applied to this connector are delayed and routed to **AUD. A OUT.**

AUD. B IN - This BNC or terminal strip connector serves as one of two AES or S/PDIF digital signal stream inputs to the product. Signals applied here are fed to the time delay and to the clock generation circuitry for the module. In either connector version, the signal can be balanced, unbalanced, 75 Ohm terminated, or 110 Ohm terminated. Signals applied to this connector are delayed and routed to **AUD. B OUT.**

AUD. A OUT - This BNC or terminal strip connector serves as one of two AES or S/PDIF digital signal stream outputs from the product. The clock embedded in this signal is a reclocked version of that extracted from **AUD. A IN**. In either connector version, the signal can be balanced, unbalanced, 75 Ohm terminated, or 110 Ohm terminated.

AUD. B OUT - This BNC or terminal strip connector serves as one of two AES or S/PDIF digital signal stream outputs from the product. The clock embedded in this signal is a reclocked version of that extracted from **AUD. B IN**. In either connector version, the signal can be balanced, unbalanced, 75 Ohm terminated, or 110 Ohm terminated.

Terminal Strip Wiring - The following numbering convention applies to the input connector and the output connector of the 507146-00 version module. Number 1 is the leftmost contact, number 5 the rightmost contact:

Pin #	Description
1	+ASTREAM
2	-ASTREAM
3	GROUND (shared)
4	+BSTREAM
5	-BSTREAM

Rear Panel Control

The delay values stored in the module can be entered and recalled via the two switches on the rear of the TimeCache module. This section describes the utilization of these switches.

SWA - Switch A is used to select the parameter to be adjusted by switch B. These are the parameters and their corresponding switch positions:

Table 1: SWA Positions and Their Functions

Sw. Pos.	Function Selected
0	Set milliseconds of time delay.
1	Set 10's of milliseconds of time delay.
2	Set 100's of milliseconds of time delay.
3	Set seconds of time delay.
4	Set 10's of seconds of time delay.
5	Set stream to be adjusted (1 for A, 2 for B, 0 for both)
6-D	Unused.
E	Set EEPROM reg. in which to save delay.
F	Recall time delay from EEPROM register.

SWB - Switch B expresses the numeric value of the parameter pointed to by Switch A. If Switch A enters and leaves any mode without Switch B being changed, the parameter value stored in RAM for that mode will not be influenced by the switch value. If Switch B is changed, the parameter pointed at by Switch A will take on the value of Switch B until Switch A is changed to another setting. Here is an example of how to set the three most significant nibbles of the time delay to zero when Switch B is initially set to '0':

1) set switch A to position 7,

2) change switch B to any value other than zero,

3) set switch B to zero,

4) set switch A to position 6,

5) change switch B to any value other than zero,

6) set switch B to zero,

7) set switch A to position 5,

8) change switch B to any value other than zero,

9) set switch B to zero.

In other words, to tell the module you want to *change* a value you must *change* switch B.

During time delay entries, Switch B's value expresses a decimal number. The values are limited such that choosing switch positions A through F will result in a value of 9.

Determining Time Delay Settings

The time delay settings are entered and stored as decimal numbers which directly indicate the delay which will be applied to the audio input signal before that signal leaves the audio output jack. The module has an intrinsic processing delay of 1.5 audio samples, so entering delays of 0 will result in delays of 1.5 audio sample periods through the module. The time delay number is entered into the module starting with the most significant digit (SWA set to position 4), even if the value of this nibble is zero. If two adjacent nibbles require the same value to be entered , it is necessary to move SWB to another position and back again; otherwise, the module will think you don't want to change that register to something other than it's original value.

When using the module to 'fine tune' signal re-entry timings, it is often easier to monitor the time delay output relative to some 'correctly' timed signal and adjust the time delay until a satisfactory synchronization is achieved. Time delay settings beyond the maximum delay allowed by the memory size and sample rate are automatically limited to the maximum delay available from the installed memory. The following indicates maximum values for each memory option.

Table 2: Memory Options and Resulting Maximum Delays

Sample Rate (KHz)	Maximum Delay(secs)	Maximum Sw. Setting
32	32.768	32768
44.1	23.777	23777
48	21.845	21845

The most significant digit in the 'Switch Settings in Hexadecimal' column would be entered while SWA is set to position 4, the second most significant digit entered with SWA set to position 3, etc.

Parameter Storage

The present operating delay value can be stored to one of nine EEPROM registers by setting SWA to position E and setting SWB to any value from 1 to 9. The storage to EEPROM occurs when SWA is then moved OUT of position E. If SWB is set to any value except 1-9, moving SWA out of position E will NOT result in parameter storage to EEPROM. Note that separate storage locations exist for stream A and stream B parameters(9 for each), but that stream A and B parameters are stored and recalled simultaneously. Setting SWB to any value except 1-9 will result in a delay register setting of 9.

Parameter Recall

The present operating delay value can be recalled from one of nine EEPROM by setting SWA to position F and setting SWB to any value from 1 to 9. As SWB is changed, the modules delay will reflect the parameters previously stored in the corresponding EEPROM register. Setting SWB to any value except 1-9 will result in a delay register setting of 9. The module can automatically load any parameter set upon power application if SWA is moved *OUT of* position F after the desired parameter set has be selected with SWB.

Specifications

Audio Input Standard	AES3-1992, S/PDIF
Audio Input Connector	Pluggable Terminal Strip (507146-10) BNC female (507146-00)
Audio Input Impedance	75 Ohms, 110 Ohms, or >2000 Ohms
Audio Input Range	Source must be within 200 meters of input when using Belden 8281 or equiv.
Audio Output Standard	SMPTE 259M
Audio Output Connector	Pluggable Terminal Strip (507146-10) BNC female (507146-00)
Audio Output Jitter	<10 nsec. peak to peak
Minimum Time Delay	1.5 Audio Sample Clock Periods
Maximum Time Delay	sample rate dependent: 32 KHz 32.768 sec. 44.1 KHz 23.777 sec. 48 KHz 21.845 sec.
Time Delay Adj. Resolution	1 msec. (rounded to nearest sample period)
Power Consumption	5V, <1.5A 8V, <0.05A -8V, <0.05A
Operating Temperature Range	0 to 50 C, non-condensing
Operating Humidity Range	0 to 95% RH